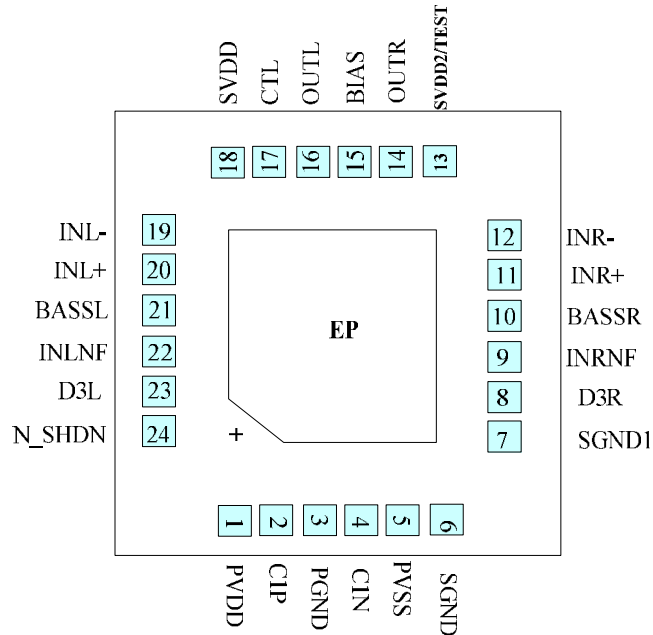


n 引脚信息



n 引脚定义

PIN	NAME	FUNCTION
1	PVDD	Charge-Pump Power-Supply Input. Bypass to PGND with 1uF.
2	C1P	Positive Flying Capacitor Connection. Connect a 1uF capacitor between C1P and C1N.
3	PGND	Power Ground. Connect PGND and SGND together at the system ground plane.
4	C1N	Negative Flying Capacitor Connection. Connect a 1uF capacitor between C1P and C1N.
5	PVSS	Negative Charge-Pump Output. Bypass to PGND with 1uF.
6	SGND	Signal Ground. Connect PGND and SGND, SGND1 together at the system ground plane.
7	SGND1	Signal Ground. Connect PGND and SGND, SGND1 together at the system ground plane.
8	D3R	3D control pin.
9	INRNFB	Right channel feedback.
10	BASSR	Right channel Bass control output.
11	INR+	Right Positive Polarity Input
12	INR-	Right Negative Polarity Input
13	SVDD2 /TEST	Signal Path Power-Supply Input. Bypass to PGND with 1uF. Connect directly to PVDD.
14	OUTR	Right Direct Drive Output
15	BIAS	Internal Supply Node. Bypass to PGND with 0.1uF.
16	OUTL	Left Direct Drive Output
17	CTL	3D and Bass function control.
18	SVDD	Signal Path Power-Supply Input. Bypass to PGND with 1uF. Connect directly to PVDD.
19	INL-	Left Negative Polarity Input
20	INL+	Left Positive Polarity Input
21	BASSL	Left channel Bass control output.
22	INLNFB	Left channel feedback.
23	D3L	3D control pin.
24	N_SHDN	Active-Low Shutdown. Drive N_SHDN high for normal operation.
	EP	Exposed Pad. Connect at the system ground plane.

n 功能描述及应用信息

1. 模式控制

通过pin17 CTL的控制，可使HT97230进入不同的工作模式。该引脚支持两种控制方式：

(1) 电压控制方式

在CTL引脚输入一定的电压，可使HT97230进入不同的工作模式，具体如下表：

Table. 1 CTL mode control with voltage

CTL voltage	Working mode
0.8*PVDD~PVDD	CTL control with pulse
0.6*PVDD~0.8*PVDD	BASS + 3D
0.4*PVDD~0.6*PVDD	3D
0.2*PVDD~0.4*PVDD	BASS
0~0.2*PVDD	Normal

(2) 一线脉冲模式

但CTRL拉高至PVDD（如上表1），在CTRL引脚输入不同脉冲数，即可进入不同的工作模式，如下表：

Table. 2 CTL mode control with pulse

Amount of pulses	Working mode
3	BASS + 3D
2	3D
1	BASS
0,4	Normal

2. Normal Mode

增益设置：

$$AV0 = R_F/R_{IN}, (R_F = R_{F3}/(R_{F1}+R_{F2}))$$

3. Bass Mode

低音增强+3dB频率点

$$f_B = \frac{R_{F3} - 0.75 * (R_{F2} + R_{F1})}{2\pi * 0.75 * \{(R_{F2} + R_{F1})^2 + R_{F3} * (R_{F1} + R_{F2})\} * C_B}$$

4. 3D Mode

3D环绕音效功能启动+3dB频率点

$$f_{3D} = \frac{1}{2\pi(R_{3D} + \frac{R_{F1} + R_{F2}}{R_{F1} + R_{F2} + R_{F3}})C_{3F}} \approx \frac{1}{2\pi R_{3F} C_{3F}}$$

5. 输入滤波器

输入电容C_{IN}与输入电阻R_{IN}组成高通滤波器，其截止频率影响低频信号的输入。截止频率：

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}};$$

6. 输入电容C_{IN}，输入电阻R_{IN}，反馈电阻R_F

输入电容C_{IN}，输入电阻R_{IN}，反馈电阻R_F应尽可能使用高精度器件，以使芯片发挥更优秀的失真、信噪比等性能。

n PCB Layout

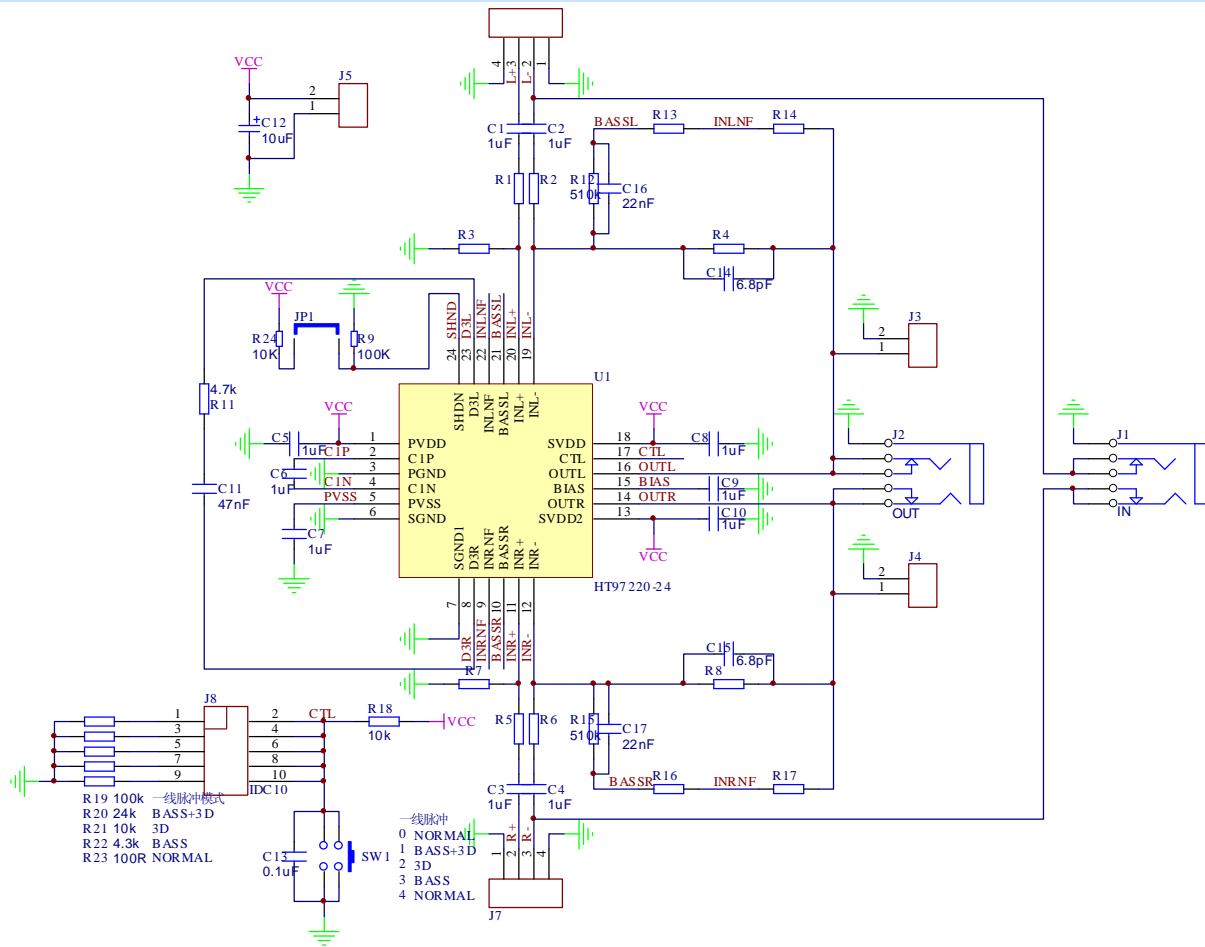
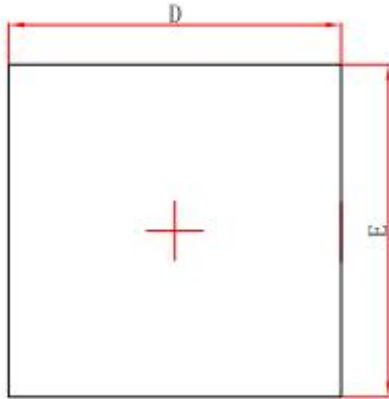


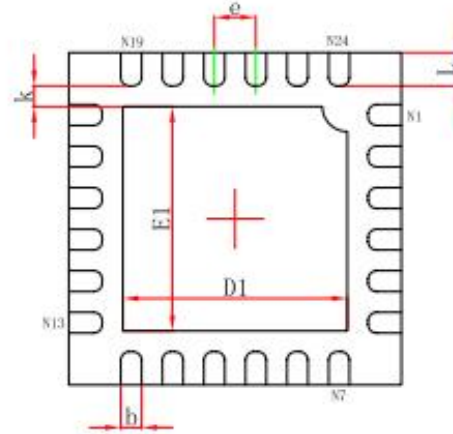
Fig. 1 Schematic Diagram of HT97230 Demo Board

n 封装外形

QFNWB4×4-24L (P0.50T0.75/0.85) PACKAGE OUTLINE DIMENSIONS



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020

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